REMARKS

Claims 1-9 are currently pending in this application. Claims 1-4 have been amended for clarity without further limitation. In view of the above amendments and following remarks, applicants respectfully submit that the application is in condition for allowance. Applicants therefore, respectfully request reexamination, reconsideration and allowance of the application.

The Examiner rejected claims 1-9 under 35 U.S.C. 103(a) as being obvious over Porterfield (U.S. Patent 6,141,715) in view of Alzien et al., (U.S. Patent 5,987,555). The Examiner admits that Porterfield fails to disclose assigning priority for ownership o the PCI bus to the master based on availability of data. The Examiner alleges however that Alzien discloses that once the data is available the PCI arbiter provides a level of arbitration priority to the PCI master. Applicant respectfully traverses this rejection.

Independent claim 1 recites a method for assigning ownership of a peripheral component interconnect (PCI) bus comprised in part by "determining if data associated with the target is available; and assigning a first priority level for ownership of the PCI bus to the master based on availability of the data." Applicants respectfully submit that the cited references, alone or in combination do not disclose or suggest the recited limitation.

Rather, in the system of Alzien when a delayed read operation is established by a particular PCI master, "bridge logic unit 102 provides an indication to the PCI arbiter 804 indicating the pending delayed read operation. PCI arbiter 804 responsively prevents the PCI master from obtaining ownership of PCI bus 114. When the delayed read data is obtained and available in transient read buffer 416, bridge logic unit 102 provides a further indication to PCI arbiter 804, which responsively provides a normal level of arbitration priority to the PCI master to allow the reattempted read operation." (Alzien, col. 23, lines 13-22; underlining added for emphasis only). Thus, in the system of Alzien, the arbiter provides a normal level of arbitration priority only when the data is available rather than determining the availability of data and assigning a priority level to the master based on that availability as recited in claim 1 (underlining added for emphasis only).

Applicants therefore respectfully submit that claim 1 recites a novel and unobvious method over the cited references and is therefore allowable. Applicants further submit that claims 2-9 that depend directly of indirectly from claim 1 are allowable as is claim 1 and for additional limitations recited therein.

It is therefore respectfully submitted that pending claims 1-9 are in condition for allowance, and an early notice of allowance is respectfully requested.

Attached hereto is a marked-up version of the changes made to the above-identified application by the current amendment. The attached page is captioned "**Version with markings to show changes made**."

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

Please amend claims 1-4 to read as follows.

1. (Twice Amended) A method of assigning ownership of a peripheral component interconnect (PCI) bus, the method including:

identifying a target requested by a master;

determining if data associated with the target is available; and

assigning a first priority level for ownership of the PCI bus to the master based on availability of the data.

2. (Amended) The method of Claim 1, [wherein] further comprising assigning the master a MEDIUM priority level after the master requests a target[, the master is assigned a MEDIUM priority].

3. (Amended) The method of Claim 1, wherein assigning a first priority level for ownership of the PCI bus to the master based on availability of the data comprises assigning a LOW priority level to the master if the data is not available[, then the master is assigned a LOW priority].

4. (Amended) The method of Claim 1, wherein assigning a first priority level for ownership of the PCI bus to the master based on availability of the data comprises assigning a HIGH priority level to the master if the data is available[, then the master is assigned a HIGH priority].

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